WHAT IS CLAIMED IS:

1. A method of programming a plurality of non-volatile memory cells to have a plurality of threshold voltage levels, the method comprising:

programming the memory cells with at least one voltage pulse;

after at least one voltage pulse, continuing programming if no memory cell has reached or exceeded a first predetermined threshold voltage level, the first predetermined threshold voltage level representing a first set of data bits;

inhibiting programming of any memory cell that has reached or exceeded the first predetermined threshold voltage level;

determining whether all memory cells selected to store the first set of data bits have reached or exceeded the first predetermined threshold voltage level;

if at least one memory cell selected to store the first set of data bits has not reached or exceeded the first predetermined threshold voltage level, continuing programming of uninhibited memory cells;

if all memory cells selected to store the first set of data bits have reached or exceeded the first predetermined threshold voltage level, determining whether all memory cells selected to store second or third sets of data bits have reached or exceeded the first predetermined threshold voltage level;

if at least one memory cell selected to store second or third sets of data bits has not reached or exceeded the first predetermined threshold voltage level, continuing programming uninhibited memory cells until all memory cells selected to store second or third sets of data bits have reached or exceeded the first predetermined threshold voltage level; and

if all memory cells selected to store second or third sets of data bits have reached or exceeded the first predetermined threshold voltage level, continuing programming all memory cells selected to store second or third sets of data bits.

2. The method of Claim 1, further comprising receiving a plurality of data bits corresponding to a plurality of predetermined threshold voltage levels to be programmed in the memory cells.

3. The method of Claim 1, further comprising selecting a group of memory cells to program.

4. The method of Claim 3, wherein the selected group comprises over 1000 cells.

5. The method of Claim 1, wherein the non-volatile memory cells are configured in a NAND-type array.

6. The method of Claim 1, wherein the non-volatile memory cells are configured in a NOR-type array.

7. The method of Claim 1, wherein the non-volatile memory cells form an electrically-erasable, programmable read only memory (EEPROM).

8. The method of Claim 1, wherein the non-volatile memory cells form a flash memory.

9. The method of Claim 1, wherein programming comprises applying a voltage pulse with a predetermined amplitude.

10. The method of Claim 1, wherein programming comprises storing charge on a floating gate transistor in each uninhibited memory cell.

11. The method of Claim 1, wherein continuing programming if no memory cell has reached or exceeded a first predetermined threshold voltage level comprises applying a voltage pulse to the memory cells with an amplitude higher than an amplitude of a previous voltage pulse.

12. The method of Claim 1, further comprising determining whether any memory cell has reached or exceeded a first predetermined threshold voltage level.

13. The method of Claim 12, wherein determining whether memory cells have reached or exceeded a first predetermined threshold voltage level comprises applying a first verify voltage to the memory cells and determining whether the memory cells are activated.

14. The method of Claim 1, wherein inhibiting programming of any memory cell that has reached or exceeded the first predetermined threshold voltage level comprises:

inhibiting programming of memory cells selected to store the first set of data bits during a remainder of the method; and

inhibiting programming of memory cells selected to store second or third sets of data bits during a first programming period.

15. The method of Claim 1, wherein determining whether all memory cells selected to store second or third sets of data bits have reached or exceeded the first predetermined threshold voltage level comprises applying a first verify voltage to the memory cells and determining whether the memory cells are activated.

16. The method of Claim 1, further comprising:

after at least one voltage pulse, continuing programming of uninhibited memory cells if no memory cell has reached or exceeded a second predetermined threshold voltage level, the second predetermined threshold voltage level representing the second set of data bits;

inhibiting programming of any memory cell that has reached or exceeded the second predetermined threshold voltage level;

determining whether all memory cells selected to store second or third sets of data bits have reached or exceeded a second predetermined threshold voltage level;

if at least one memory cell selected to store the second or third sets of data bits has not reached or exceeded the second predetermined threshold voltage level, continuing programming of uninhibited memory cells;

if all memory cells selected to store the second or third sets of data bits have reached or exceeded the second predetermined threshold voltage level,

determining whether all memory cells selected to store the third set of data bits have reached or exceeded the second predetermined threshold voltage level;

if at least one memory cell selected to store the third set of data bits has not reached or exceeded the second predetermined threshold voltage level, continuing programming uninhibited memory cells selected to store the third set of data bits until all memory cells selected to store the third set of data bits have reached or exceeded the second predetermined threshold voltage level; and

if all memory cells selected to store the third set of data bits have reached or exceeded the second predetermined threshold voltage level, continuing programming all memory cells selected to store the third set of data bits.

17. The method of Claim 1, wherein the memory cells are coupled to a word line.

18. The method of Claim 1, further comprising inhibiting programming of memory cells that are selected to store a fourth set of data bits.

19. The method of Claim 1, further comprising repeating the method for another group of memory cells.

20. A method of using a plurality of non-volatile memory cells, the method comprising:

storing charge in the memory cells;

continuing storing charge in the memory cells if no memory cell has reached or exceeded a first predetermined charge level, the first predetermined charge level representing at least two data bits;

inhibiting storing charge in any memory cell that has reached or exceeded the first predetermined charge level;

determining whether all memory cells selected to store the first predetermined charge level have reached or exceeded the first predetermined charge level;

if at least one memory cell selected to store the first predetermined charge level has not reached or exceeded the first predetermined charge level, continuing storing charge in uninhibited memory cells;

if all memory cells selected to store the first predetermined charge level have reached or exceeded the first predetermined charge level, determining whether all memory cells selected to store second or third predetermined charge levels have reached or exceeded the first predetermined charge level; and

if at least one memory cell selected to store second or third predetermined charge levels has not reached or exceeded the first predetermined charge level, continuing storing charge in uninhibited memory cells until all memory cells selected to store second or third predetermined charge levels have reached or exceeded the first predetermined charge level.

21. The method of Claim 20, further comprising:

if all memory cells selected to store second or third predetermined charge levels have reached or exceeded the first predetermined charge level, continuing storing charge in all memory cells selected to store second or third predetermined charge levels.

22. The method of Claim 20, wherein each memory cell comprises at least one floating gate transistor configured to store charge.

23. A method of programming a plurality of non-volatile memory cells, the memory cells comprising a first set of one or more memory cells selected to store a charge level equal to or greater than a first predetermined charge level corresponding to a first set of data bits, a second set of one or more memory cells selected to store a charge level equal to or greater than a second predetermined charge level corresponding to a second set of data bits and a third set of one or more memory cells selected to store a charge level equal to or greater than a third predetermined charge level corresponding to a third set of data bits, the method comprising:

simultaneously storing charge in the first, second and third sets of memory cells;

continuing storing charge in the memory cells if no memory cell has reached or exceeded the first predetermined charge level;

inhibiting storing charge of any memory cell in the first, second and third sets that has reached or exceeded the first predetermined charge level;

determining whether all memory cells in the first set have reached or exceeded the first predetermined charge level; and

if at least one memory cell in the first set has not reached or exceeded the first predetermined charge level, continuing storing charge in uninhibited memory cells.

24. The method of Claim 23, further comprising:

if all memory cells in the first set have reached or exceeded the first predetermined charge level, determining whether all memory cells in the second and third sets have reached or exceeded the first predetermined charge level;

if at least one memory cell in the second or third sets has not reached or exceeded the first predetermined charge level, continuing storing charge in uninhibited memory cells in the second and third sets until all memory cells in the second and third sets have reached or exceeded the first predetermined charge level; and

if all memory cells in the second and third sets have reached or exceeded the first predetermined charge level, continuing storing charge in all memory cells in the second and third sets.

25. A method of programming a plurality of non-volatile memory cells to have a plurality of threshold voltage levels, the method comprising:

programming the memory cells with at least one voltage pulse;

after at least one voltage pulse, continuing programming if no memory cell has reached or exceeded a first predetermined threshold voltage level, the first predetermined threshold voltage level representing a first set of data bits;

inhibiting programming of any memory cell that has reached or exceeded the first predetermined threshold voltage level;

determining whether all memory cells selected to store the first set of data bits have reached or exceeded the first predetermined threshold voltage level;

if at least one memory cell selected to store the first set of data bits has not reached or exceeded the first predetermined threshold voltage level, continuing programming of uninhibited memory cells;

if all memory cells selected to store the first set of data bits have reached or exceeded the first predetermined threshold voltage level, determining whether any memory cell has reached or exceeded a second predetermined threshold voltage level, the second predetermined threshold voltage level representing a second set of data bits; and

inhibiting programming of any memory cell that has reached or exceeded the second predetermined threshold voltage level and continuing programming of uninhibited memory cells.

26. The method of Claim 25, further comprising:

determining whether all memory cells selected to store the second or third sets of data bits have reached or exceeded the second predetermined threshold voltage level;

if all memory cells selected to store the second or third sets of data bits have reached or exceeded the second predetermined threshold voltage level, determining whether all memory cells selected to store the third sets of data bits have reached or exceeded the third predetermined threshold voltage level; and

inhibiting programming of any memory cell that has reached or exceeded the third predetermined threshold voltage level and continuing programming of uninhibited memory cells.

27. A method of using a plurality of non-volatile memory cells, the method comprising:

storing charge in the memory cells;

continuing storing charge in the memory cells if no memory cell has reached or exceeded a first predetermined charge level, the first predetermined charge level representing at least two data bits;

inhibiting storing charge in any memory cell that has reached or exceeded the first predetermined charge level;

determining whether all memory cells selected to store the first predetermined charge level have reached or exceeded the first predetermined charge level;

if at least one memory cell selected to store the first predetermined charge level has not reached or exceeded the first predetermined charge level, continuing storing charge in uninhibited memory cells;

if all memory cells selected to store the first predetermined charge level have reached or exceeded the first predetermined charge level, determining whether any memory cell selected to store second or third predetermined charge levels has reached or exceeded the second predetermined charge level;

inhibiting storing charge in any memory cell that has reached or exceeded the second predetermined charge level; and

if no memory cell selected to store second or third predetermined charge levels has reached or exceeded the second predetermined charge level, continuing storing charge in uninhibited memory cells.

28. The method of Claim 27, further comprising:

determining whether all memory cells selected to store the second predetermined charge level have reached or exceeded the second predetermined charge level;

if at least memory cell selected to store the second predetermined charge level has not reached or exceeded the second predetermined charge level, continuing storing charge in uninhibited memory cells; and

if all memory cells selected to store the second predetermined charge level have reached or exceeded the second predetermined charge level, determining whether any memory cell selected to store the third predetermined charge level has reached or exceeded the third predetermined charge level;

if at least memory cell selected to store the third predetermined charge level has not reached or exceeded the second predetermined charge level, continuing storing charge in all memory cells selected to store the third predetermined charge level, until all memory cells selected to store the third predetermined charge level have reached or exceeded the third predetermined charge level.

29. The method of Claim 27, wherein each memory cell comprises at least one floating gate transistor configured to store charge.

30. A method of programming a plurality of non-volatile memory cells, the memory cells comprising a first set of one or more memory cells selected to store a charge level equal to or greater than a first predetermined charge level corresponding to a first set of data bits, a second set of one or more memory cells selected to store a charge level equal to or greater than a second predetermined charge level corresponding to a second set of data bits and a third set of one or more memory cells selected to store a charge level equal to or greater than a third predetermined charge level corresponding to a third set of data bits, the method comprising:

simultaneously storing charge in the first, second and third sets of memory cells;

continuing storing charge in the memory cells if no memory cell has reached or exceeded the first predetermined charge level;

inhibiting charging of any memory cell in the first, second and third sets that has reached or exceeded the first predetermined charge level;

determining whether all memory cells in the first set have reached or exceeded the first predetermined charge level;

if at least one memory cell in the first set has not reached or exceeded the first predetermined charge level, continuing storing charge in uninhibited memory cells;

if all memory cells in the first set have reached or exceeded the first predetermined charge level, determining whether any memory cell in the second set has reached or exceeded the second predetermined charge level; and

if at least one memory cell in the second set has not reached or exceeded the second predetermined charge level, continuing storing charge in uninhibited memory cells in the second and third sets.

31. A memory device comprising:

a plurality of non-volatile memory cells, the memory cells comprising:

a first set of one or more memory cells selected to store a charge equal to or greater than a first predetermined charge level corresponding to a first set of data bits;

a second set of one or more memory cells selected to store a charge equal to or greater than a second predetermined charge level corresponding to a second set of

data bits, wherein the memory device is configured to simultaneously program the first and second sets of memory cells and inhibit programming of any memory cell that reaches or exceeds the first predetermined charge level until all memory cells in the first set have reached or exceeded the first predetermined charge level.

32. The memory device of Claim 31, wherein the memory device is further configured to continue programming until all memory cells in the second set have reached or exceeded the first predetermined charge level.

33. The memory device of Claim 31, wherein the memory device is further configured to verify whether memory cells have reached or exceeded the first predetermined charge level by applying a first test voltage to the memory cells.

34. The memory device of Claim 31, wherein the memory device is further configured to continue programming until all memory cells in the second set have reached or exceeded the second predetermined charge level.

35. The memory device of Claim 34, wherein the memory device is further configured to verify whether memory cells have reached or exceeded the second predetermined charge level by applying a second test voltage to the memory cells.

36. The memory device of Claim 31, wherein each memory cell comprises a floating gate transistor configured to store charge.

37. The memory device of Claim 31, wherein the memory cells are organized in a plurality of rows and columns.

38. The memory device of Claim 31, wherein the first and second sets of memory cells are within an activated row of memory cells.

39. A method of programming a plurality of non-volatile memory cells, the method comprising:

storing charge in a first set and a second set of memory cells;

continuing storing charge in the memory cells if no memory cell has reached or exceeded a first predetermined charge level, the first predetermined charge level representing at least two data bits;

inhibiting storing charge in any memory cell that has reached or exceeded the first predetermined charge level;

determining whether all memory cells in the first set of memory cells have reached or exceeded the first predetermined charge level;

if at least one memory cell in the first set has not reached or exceeded the first predetermined charge level, continuing storing charge in uninhibited memory cells; and

if all memory cells in the first set have reached or exceeded the first predetermined charge level, continuing storing charge in the first set of memory cells.

40. The method of Claim 39, wherein the first set of memory cells have a first initial charge level, and the second set of memory cells have a second initial charge level, wherein the second initial charge level is higher than the first initial charge level, and the predetermined charge level is higher than both the first and second initial charge levels.

41. A method of programming a plurality of non-volatile memory cells in parallel from a common threshold level into at least first and second threshold levels as designated by data being stored in the memory cells, the method comprising:

applying programming conditions to all of the plurality of memory cells designated for the first and second threshold levels;

terminating application of the programming conditions to individual ones of the plurality of memory cells designated for the first and second threshold levels as the cells designated for the first and second threshold levels individually reach said first threshold level;

after those of the memory cells designated for the first threshold level have all reached the first threshold level, applying programming conditions to those of the plurality of memory cells designated for the second threshold level; and

terminating application of the programming conditions to individual ones of the plurality of memory cells designated for the second threshold level as the cells designated for the second threshold level individually reach said second threshold level.

42. The method of Claim 41, wherein applying programming conditions to those of the plurality of memory cells designated for the second threshold level commences after all those of the memory cells designated for the second threshold level have reached said first threshold level.

43. The method of claim 41, wherein the common threshold level is also a programmed level designated by the data being stored in the memory cells and those of the plurality of the memory cells that are designated for the common level are locked out from receiving programming conditions.

44. A means for storing data comprising:

a plurality of non-volatile memory cells, the memory cells comprising:

a first set of one or more memory cells selected to store a charge equal to or greater than a first predetermined charge level corresponding to a first set of data bits;

a second set of one or more memory cells selected to store a charge equal to or greater than a second predetermined charge level corresponding to a second set of data bits, wherein the memory device is configured to simultaneously program the first and second sets of memory cells and inhibit programming of any memory cell that reaches or exceeds the first predetermined charge level until all memory cells in the first set have reached or exceeded the first predetermined charge level.

45. The means for storing data in Claim 44, further comprising a means for selecting the first and second sets of memory cells for programming.